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RESPONSE UNDER 37 C.F.R. §1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2306

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#18
Date
8/10/99

In re Patent Application of
Johannes Roelof Gerardus de Vries
Serial No.: 08/422,264
Filed: April 14, 1995

New York, New York
Date: August 11, 1997
Group Art Unit: 2306
Examiner: R. Dolan

For: DATA PROCESSING CIRCUIT, MULTIPLIER UNIT WITH PIPELINE, ALU AND SHIFT REGISTER UNIT FOR USE IN A DATA PROCESSING CIRCUIT

Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

AMENDMENT PURSUANT TO 37 C.F.R. §1.116

Sir:

In response to the final Office Action mailed May 9, 1997, please reconsider the above-identified application amended as follows and in light of the following remarks:

IN THE CLAIMS:

Please cancel claims 4 and 19 without prejudice.

Please amend the claims as follows:

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1. (Twice Amended) A circuit for processing integer data for graphic image processing applications, comprising:

a multiplier unit having a pipeline for multiplying integer data words of 8 bits or multiples thereof, the pipeline being adjustable to the length of the integer data words to be multiplied;

an arithmetic logic unit (ALU) for performing arithmetic operations on integer data words of 8 bits or